MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/2020

EEE3196 – INTEGRATED VLSI SYSTEMS

(EE)

28 FEBRUARY 2020
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 7 pages with 4 questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\Phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\,R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) Given a CMOS inverter with the following parameters:
$k'_n = 110\ \mu A/V^2$, $k'_p = -30\ \mu A/V^2$, $V_{Tn} = |V_{Tp}| = 0.4$ V, $V_{DD} = 3$ V, $V_{GS} = 3$ V, $(W/L)n = 2$, $(W/L)p = 3$ and $C_L = 30$ pF.

(i) Using the average current (I_{avg}) method, find the high-to-low propagation delay (t_{PHL}). [8 marks]

(ii) Using the average on-resistance (R_{on}) method, find the high-to-low propagation delay (t_{pHL}). [4 marks]

(iii) Calculate the low-to-high propagation delay (t_{pLH}) and the total propagation delay (t_p). [4 marks]

(iv) Calculate the Power-Delay-Product (PDP) of the CMOS inverter, assuming that the frequency, f = 10 MHz and the static current, I_{st} is equivalent to 30 μA. [4 marks]

(b) Figure Q1 shows the graph of technology scaling against energy and power supply.

(i) Critic and comment on the graph. [3 marks]

(ii) List out TWO ways on how the energy can be dissipated. [2 marks]

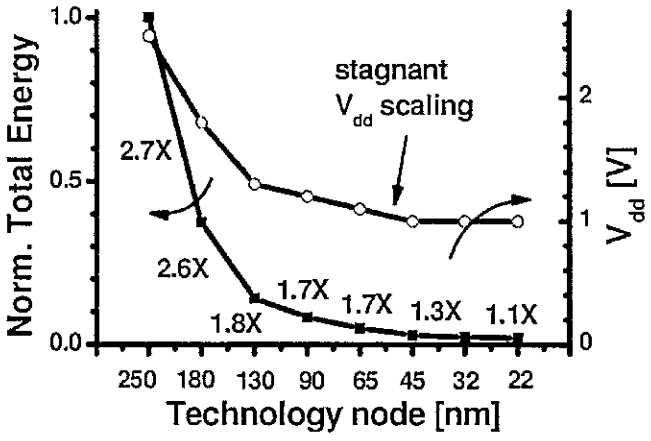


Figure Q1

Continued...

Question 2

(a) Consider a uniform metal-1 Aluminium wire with a length of 20 μm and a width of 4 μm. Assume a sheet resistance value of 80 mΩ/square and the typical interwire capacitance values are:

Area capacitance = 30 aF/μm^2

Fringing capacitance = 40 aF/μm

(i) Calculate the total lumped resistance with this wire. [2 marks]

(ii) Calculate the total capacitance associated with this wire. [6 marks]

(b) Consider a pair of Aluminium wires; Line 1 and 2 as shown in Figure Q2, each with a capacitance to ground value of 10 pF. Both wires have a 1 pF coupling capacitance between them. A square pulse of 2 V voltage source is connected to Line 1.

(i) Calculate the noise pulse voltage level that can be reached on Line 2. [4 marks]

(ii) Describe the impact of the interwire capacitance. [2 marks]

(iii)Propose THREE methods to battle this capacitance effect which occurred between two wires. [6 marks]

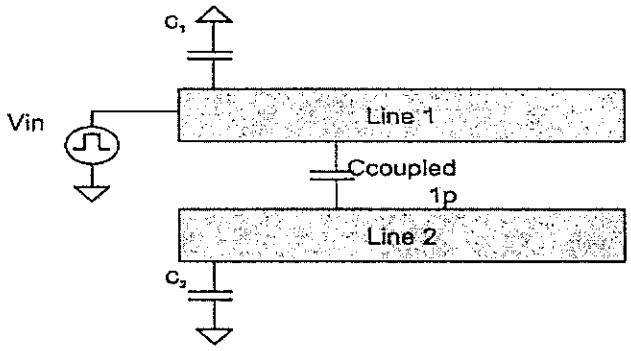


Figure Q2

(c) In any circuit, current flowing through resistive wires will results in ohmic voltage drop that degrades signal levels. Hence it is important to have an efficient on-chip power distribution network.

(i) Describe the impact of resistance in power supply distribution. [3 marks]

(ii) Recommend ONE method to minimize noise due to resistance in the power distribution network. [2 marks]

Continued...

Question 3

(a) Given the following function:

$$Y = \overline{A + B.C.D}$$

(i) Design and sketch the circuit for this function Y using minimal conventional static CMOS transistors. [6 marks]

(ii) From part (i), modify the circuit using:

a. depletion-load NMOS
b. pseudo-NMOS
c. dynamic logic [6 marks]

(iii)From part (ii), compare the circuits using depletion-load NMOS and pseudo-NMOS. Which is better and why?

[2 marks]

(b) Figure Q3(a) below shows an AND gate designed using Pass-Transistor Logic (PTL) properties.

(i) Describe the operation of the AND gate, when B is logic "1".

[5 marks]

(ii) Explain the advantage of PTL compared to fully complementary CMOS logic. [2 marks]

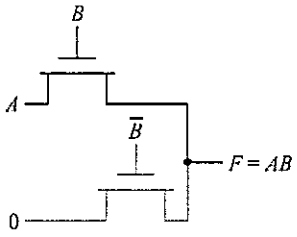


Figure Q3(a)

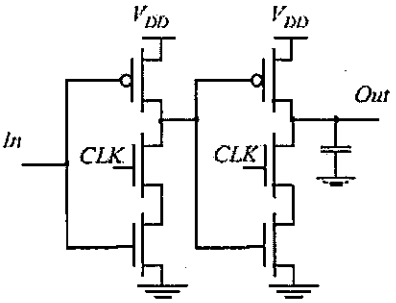


Figure Q3(b)

(c) Figure Q3(b) shows the circuit of True Single Phase Clocked (TSPC) latch.

(i) Describe the operation of the TSPC latch when the CLK is high.

[2 marks]

(ii) Modify the circuit to become negative latch TSPC.

[2 marks]

Continued...

Question 4

(a) Given an 8-bit ripple carry adder (RCA) with different delays as listed below:
$t_{carry0\rightarrow1} = 320ps$, $t_{carry1\rightarrow0} = 350ps$,
$t_{sum0\rightarrow1} = 420ps$, $t_{sum1\rightarrow0} = 450ps$.

(i) Find the worst case delay t_{adder}.

[3 marks]

(ii) Give an example of input value that will trigger this worst case delay.

[2 marks]

(b) Figure Q4(a) shows a conventional 6-transistor CMOS SRAM (Static Random Access Memory) cell.

(i) Describe the operation of this memory cell when it writes a "0" in the cell, assuming "1" is initially stored in the cell.

[6 marks]

(ii) Modify the circuit to become Resistance-load SRAM cell.

[4 marks]

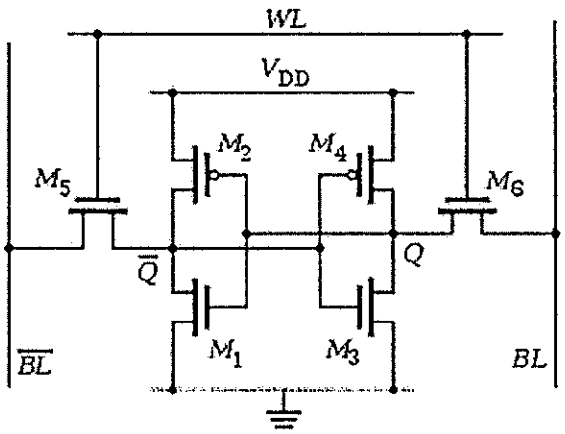


Figure Q4(a)

Continued...

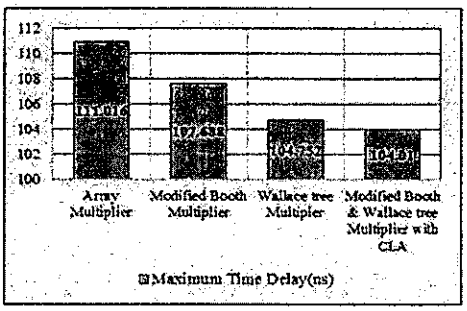
(c) Figure Q4(b) shows the comparison between different multipliers on maximum time delay and Look-Up Tables (LUTs) utilized.

(i) Comment on the graph.

[4 marks]

(ii) Wallace tree Multiplier is an efficient hardware implementation of a multiplier. However, it will still have its own advantages and disadvantages. Elaborate on the pros and cons of the Wallace tree Multiplier.

[6 marks]



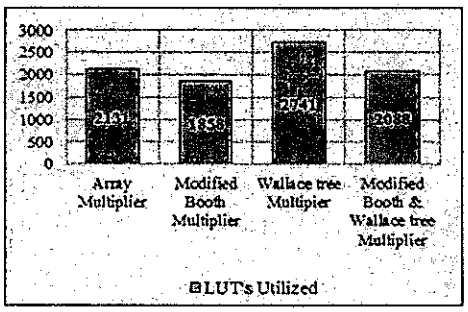


Figure Q4(b)

End of Paper